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Technical Datasheet

takeMS BD2048TEC850

Description

These Memory devices are JEDEC standard registered DIMM modules, based on CMOS DDR SDRAM technology.
These devices consist of CMOS DDR SDRAMs in TSOP or FBGA packages on a 184-pin glass epoxy substrate.The memory array is designed with Double Data Rate (DDR) Synchronous DRAMs for server applications.
The pipelined, multibanked architecture of DDR SDRAMs allows for concurrent operation, thereby providing high, effective bandwidth.
Decoupling capacitors are mounted on the PCB board in parallel for each DDR SDRAM, which provides proper voltage supply impedance over the whole frequency range of operations, in accordance with JEDEC specifications. These modules feature Serial Presence Detect (SPD) based on a serial EEPROM device.

Features
184-pin registered DDR SDRAM
JEDEC Standard 184pin DIMM 2.5V +/- 0.2V VDD & VDDQ Power supply
Auto Refresh (CBR) and Self Refresh Mode
Programmable Burst Length
Fully differential clock operations
Serial Presence Detect (SPD) with EEPROM
Module layout is based on JEDEC standard routing guidelines
Impedance controlled 6-layer PCB Technology
JEDEC standard form factor
Internal four bank operations
single pulsed data for write RAS
Operating Temperature 0°C ~ 75°C

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Technical details

- **2048 MB longdimm module**
- **128Mx4 IC organisation**
- **x72 module organisation**
- **333MHz / PC 2700**
- **double sided / 32 ICs (+ECC and register)**
- **CAS Latency 2,5 at max. memclock**

For pin configuration please check www.takems.com/support/index.php

If you have any questions regarding our products you can contact us via email: info@takems.com

Order-No.: **BD2048TEC850**

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